APPENDIX

PENDING CLAIM

(Claims 1-8 have been cancelled.)

9. A microprocessor, comprising:

a central processing unit with an instruction set including three-byte instructions;

a memory for storing the instructions, wherein the instructions are stored contiguously; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein each of said instructions is supplied in a single fetch operation.

10. The microprocessor of claim 9, wherein said instruction set further includes two-byte instructions and one-byte instructions.

11. The microprocessor of claim 9, wherein said memory is a one time programmable memory.

12. The microprocessor of claim 9, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

(Claims 13-24 have been cancelled.)

25. A method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte instructions, a memory for storing the instructions, and a

memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M columns, wherein M is an integer greater than one and wherein N and M are relatively prime;

programming the instruction set into the memory, wherein the instructions are stored contiguously in the memory; and

operating the interface whereby each of the instructions can be supplied from the memory to the central processing unit in a single fetch operation.

26. The microprocessor of claim 25, wherein N is equal to three and M is equal to four.

27. The microprocessor of claim 26, wherein said instruction set further includes two byte instructions and one byte instructions.

28. The microprocessor of claim 26, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

29. The microprocessor of claim 25, wherein the memory is an embedded memory of the microprocessor.

30. The microprocessor of claim 29, wherein the memory is a one time programmable memory.